

What is claimed is:

1. A speech synthesizer comprising:

a signal transform unit for receiving and transforming a series

of digital speech codes to be an analog speech signal

with its negative half cycles inverted; and

a current output unit connected to said signal transform unit

and including a first and second signal output

terminals, for receiving said analog speech signal and

outputting its positive and negative cycles currents

respectively from said first and second output

terminals.

2. A speech synthesizer according to claim 1 further

comprising a volume control unit for receiving a control signal and

generating a control bias.

3. A speech synthesizer according to claim 1 wherein said
signal transform unit controls transformation of said digital speech

codes with a most significant bit of each said digital speech code.

4. A speech synthesizer according to claim 1 wherein said
signal transform unit comprising:

a switched buffer controlled by said most significant bit of said

digital speech codes for receiving and outputting other

bits of said digital speech codes;
a switched inverter buffer controlled by an inverse of said
most significant bit of said digital speech codes for
receiving and outputting other bits of said digital
speech codes; and
a digital-to-analog converter connected to said switched buffer
and inverter buffer for transforming into said analog
speech signal.

5. A speech synthesizer according to claim 1 wherein said
current output unit comprising:
- a first switch controlled by said most significant bit of said
digital speech codes, with a first terminal connected to
said first signal output and a second terminal
connected to a high voltage;
 - a second switch controlled by an inverse of said most
significant bit of said digital speech codes, with a first
terminal connected to said second signal output and a
second terminal connected to said high voltage;
 - a first switched current source controlled by said most
significant bit of said digital speech codes, for
outputting said analog speech signal and with a first
terminal connected to said second signal output and a
second terminal connected to a low voltage; and
 - a second switched current source controlled by said most

significant bit of said digital speech codes, for
outputting said analog speech signal and with a first
terminal connected to said first signal output and a
second terminal connected to said low voltage.

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6. A speech synthesizer according to claim 1 wherein said
current output unit comprising:

a first switched current source controlled by said most

significant bit of said digital speech codes, with a first
terminal connected to said first signal output and a
second terminal connected to a high voltage;

a first switch controlled by said most significant bit of said
digital speech codes, for outputting said analog speech
signal and with a first terminal connected to said
second signal output and a second terminal connected
to a low voltage;

a second switch controlled by an inverse of said most
significant bit of said digital speech codes, with a first
terminal connected to said second signal output and a
second terminal connected to said high voltage; and

a second switched current source controlled by said most
significant bit of said digital speech codes, for
outputting said analog speech signal and with a first
terminal connected to said first signal output and a
second terminal connected to said low voltage.

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7. A speech synthesizer according to claim 1 wherein said current output unit comprising:

a first switched current source controlled by said most significant bit of said digital speech codes, with a first terminal connected to said first signal output and a second terminal connected to a high voltage;

a second switched current source controlled by said most significant bit of said digital speech codes, with a first terminal connected to said second signal output and a second terminal connected to said high voltage;

a first switch controlled by said most significant bit of said digital speech codes, for outputting said analog speech signal and with a first terminal connected to said second signal output and a second terminal connected to a low voltage; and

a second switch controlled by said most significant bit of said digital speech codes, for outputting said analog speech signal and with a first terminal connected to said first signal output and a second terminal connected to said low voltage.

8. A speech synthesizer according to claim 5 wherein said first and second switches are transistors.

9. A speech synthesizer according to claim 6 wherein said first and second switches are transistors.

10. A speech synthesizer according to claim 7 wherein said first and second switches are transistors.

11. A speech synthesizer according to claim 5 wherein said first switched current source comprising:

a first transistor with a drain connected to an output of said signal transform unit, a source connected with said low voltage, and a gate connected to its drain;

a second transistor with a gate, a drain connected to said first signal output terminal and a source connected to said low voltage; and

a first variable current controlled switch controlled by said most significant bit of said digital speech codes, with a first terminal connected to said gate of said first transistor and a second terminal connected to said gate of said second transistor for forming a current mirror composed of said first and second transistors when said first variable current controlled switch is enabled.

12. A speech synthesizer according to claim 11 said second switched current source comprising:

a third transistor with a gate, a drain connected to said first

signal output terminal and a source connected to said low voltage;

and

a second variable current controlled switch controlled by said

most significant bit of said digital speech codes, with a

5 first terminal connected to said gate of said first

transistor and a second terminal connected to said gate

of said third transistor for forming an another current

mirror composed of said first and third transistors when

said second variable current controlled switch is

10 enabled.